

Dynamic voltage restorer employing multilevel cascaded H-bridge inverter

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Soleiman Galeshi, Hossein Iman-Eini 🖾

School of Electrical and Computer Engineering, College of Engineering, University of Tehran, Tehran 111554563, Islamic Republic of Iran E-mail: imaneini@ut.ac.ir

Abstract: This study presents design and analysis of a dynamic voltage restorer (DVR) which employs a cascaded multilevel inverter with capacitors as energy sources. The multilevel inverter enables the DVR to connect directly to the medium voltage networks, hence, eliminating the series injection transformer. Using zero energy compensation method, the DVR does not need active energy storage systems, such as batteries. Since the energy storage system only includes capacitors, the control system will face some additional challenges compared with other DVR systems. Controlling the voltage of capacitors around a reference voltage and keeping the balance between them, in standby and compensation period, is one of them. A control scheme is presented in this study that overcomes the challenges. Additionally, a fast three-phase estimation method is employed to minimise the delay of DVR and to mitigate the voltage sags as fast as possible. Performance of the control scheme and estimation method is assessed using several simulations in PSCAD/EMTDC and MATLAB/SIMULINK environments, and experiments on a 7-level cascaded H-bridge converter.

1 Introduction

Together with increasing number of sensitive loads in the power networks, power quality (PQ) is becoming more important every day. There are many types of PQ problems, such as voltage sag/ swell, voltage imbalance and flicker. PQ problems cost European industries about ten billion dollars, annually [1]. A study on Mazandaran wood and paper industry (MWPI) [2], including measurement and economic analysis, revealed that interruption of production lines due to voltage sag costs about \$200,000 annually. The most common PQ problem that both industrial and commercial consumers suffer from, is voltage sag [3, 4]. Voltage sags usually originate from several sources, including faults on facility side or the utility network, reclosing the circuit breakers, and in-rush current of large electrical motors at startup. As a flexible AC transmission system (FACTS) device, dynamic voltage restorer (DVR) is employed for mitigation of voltage sags through series injection of voltage and restoring the dropped supply voltage to its normal level [5, 6]. Generally a DVR is made of four main units: measurement stage, control unit, voltage source inverter and series injection transformer; the latter one is a bulky low-frequency transformer which increases the system cost.

Huang *et al.* [7] present a DVR, designed for 220 V network, which utilises a conventional inverter with batteries as active energy storage system (ESS). Since the inverter is of 2-level conventional type, its switching frequency has to be as high as 10 kHz and a filter is needed at the output side. Another DVR model with conventional inverter is proposed in [8]. In addition to eliminate voltage sags, this model can eliminate steady-state harmonics and improve the PQ of supply voltage even if the voltage is in normal range. Employing a 2-level inverter with 10 kHz switching frequency, this DVR needs a series injection transformer to connect into the medium voltage network.

Lozano-Garcia and Ramirez [9] introduce a DVR with a direct AC-AC matrix converter. The proposed DVR system does not need any energy storage, since it draws the energy required for voltage compensation from the grid. While this topology benefits from the advantages of eliminating energy storage system, such as smaller size and lower costs, it has some negative impacts on supply network currents: the supply currents will increase during compensation and the switching distortions will be fed to the line currents. A three-leg single-phase DVR is presented in [10]. This DVR mitigates voltage sags through a single AC-AC power conversion. It uses a boost converter to mitigate voltage sags and a buck converter in case of voltage swells. Due to single stage power conversion, size of the energy storage was reduced. A 220 V prototype of this system was designed and tested. Switching frequency of the conventional converter of this system was as high as 20 kHz. Rosas-Caro et al. [11] present a three-phase pulse width modulation (PWM) voltage regulator-based DVR with only two switches and no energy storage elements. It is a compact, cost effective and reliable DVR with a simple control system. Regarding the topology that uses only two switches, this DVR requires high switching frequency, as high as 6 kHz, and an output low-pass filter. A series injection transformer is also required to connect the DVR to medium voltage networks. The experimental results of testing a 220 V prototype approve the performance of this DVR in mitigating balanced voltage sags. Since it cannot inject negative sequence, mitigation of unbalanced voltage sags is not possible.

A medium voltage DVR with cascaded H-bridge (CHB) converter has been introduced in [12]. This DVR employs multiple DQ transforms to implement its measurement and control strategy. The multiple DQ transform system allows fast and accurate operation of the DVR under harmonics and unbalanced conditions. Babaei *et al.* [13] introduce a DVR which employs a CHB multilevel converter. This DVR also includes a DC–DC converter to adjust its DC link voltage. The DC–DC converter allows for changing the DC link voltage so output voltage of the converter has the maximum possible number of levels for a wide range of voltage sags. Since the output voltage is always a well-shaped multilevel voltage, this DVR needs a very small output filter, but the extra DC–DC converter increases the power losses and system cost.

Al-Hadidi *et al.* [14, 15] introduce a DVR which employs a CHB multilevel inverter. ESS of this DVR contains capacitors and it works in reactive voltage injection mode. In this structure, all H-bridges of the CHB inverter have been considered to be ideal and completely identical, but, in reality, the converter will face different losses in the H-bridge cells (or voltage unbalance among the capacitors). To resolve this problem, the control system has to

establish voltage balance among the capacitors in all operating conditions.

Measurement unit is another critical part of the DVR and it must recognise occurrence of voltage sags and estimates the values of supply voltage and the current. A fast estimation method for unbalanced three-phase voltage systems is introduced in [16] which is able to estimate magnitude and phase of three-phase voltage/currents with maximum delay of half a cycle. This method is also employed in this paper.

In this study, the recorded data for the MWPI [2] is used as the base data for design of CHB-based DVR. According to the recorded data at the input feeder of MWPI, most of the voltage sags have a depth between 10 and 20% of nominal voltage. Now to connect the CHB-based DVR directly to 20 kV supply network and mitigate voltage sags of maximum 20% depth, a 13-level inverter with 1700 V insulated gate bipolar transistors (IGBTs) is suggested for this application. Due to the near-sinusoidal 13-level output waveform, the switching frequency is 2 kHz and a small line filter is used. Moreover, using the capacitors as energy storages, voltage sags can be successfully mitigated for the aforementioned range. Same as the practical conditions, the internal losses of the H-bridge cells are assumed to be unequal and a new control scheme is proposed to keep the voltage balance among the DC link capacitors. Using the estimation method in this paper, voltage sags are mitigated in less than half a cycle.

Section 2 discusses zero energy compensation method and the structure of CHB converter. Section 3 introduces the voltage control scheme of the converter. The employed estimation method is presented in Section 4. Simulation results are presented in Section 5. Several simulations have been performed in PSCAD/ EMTDC environment to assess the performance of the proposed DVR and its control system. Experimental results are presented in Section 6 along with corresponding MATLAB/SIMULINK simulation results. Finally, conclusions are included in Section 7.

2 Voltage restoration and the multilevel converter

2.1 Zero energy voltage restoration

As a FACTS device, DVR is installed in series with supply lines of industrial plants. Therefore, in case of voltage sag, it can inject a voltage in series with the supply voltage, restoring it to the nominal value. The compensation is possible in three different ways: post-fault, pre-fault and zero energy compensation [5]. Fig. 1 displays corresponding phasor diagrams of these methods. In post-fault mode, depicted in Fig. 1a, the injection voltage is in-phase with the source voltage, where the amplitude of load voltage is kept constant. This technique is the simplest way of compensation with the smallest amount of injection voltage, while it requires the largest amount of active power. In order to perform post-fault compensation, the measurement unit determines depth of voltage sag and phase of the source voltage. On the basis of this data, the control system will then generate a reference sinusoidal signal which is in-phase with the source voltage and its magnitude is equal to depth of voltage sag. This signal is fed to the inverter and the compensating voltage is generated based on it. The compensation voltage will be added to the source voltage and restore the load voltage to nominal value.

Fig. 1*b* illustrates pre-fault compensation. This method is employed for protection of loads that are sensitive to phase-jump. In this method, the injection voltage is calculated in a way that not only the magnitude of load voltage is restored to the nominal value, but also its phase is restored to the initial value prior to voltage sag. The injection voltage in this mode is greater than or equal to that of post-fault method, depending on phase jump. Flow of active and reactive energies also depend on phase jump during the voltage sag.

The method which is employed in this research is zero energy compensation, displayed in Fig. 1c. In this mode, the compensation voltage is injected in a way that to be orthogonal to



Fig. 1 *Different compensation techniques a* Post-fault

b Pre-fault

c Zero energy approach. Φ is the load angle, and α is the phase difference between network and DVR voltage. Phasor of DVR voltage ($V_{\rm DVR}$) is perpendicular to load current ($I_{\rm load}$)

the load current, after compensation. Therefore, active power is not transferred between the DVR and the load. This method usually requires a large injection voltage. The load will also experience active power drop and phase jump; but since no active power is required, the DVR does not need a source of active energy (e.g. batteries). This method is usually adopted for protection of high power loads. Hence, it is employed in this paper and further studied in the following paragraphs.

The estimation unit of a DVR continuously measures the source voltage of the plant and generates a signal as soon as it drops below 90% of nominal value. The compensation unit then will use the measured data for calculation of reference signal V^*_{DVR} and send it to the inverter. In zero energy compensation, the voltage of DC-link capacitors will not drop during compensation. According to the phasor diagram of zero energy compensation in Fig. 1*c*, the following equations are derived, where V_{load} is assumed to be 1 pu and is not written in the following equation

$$\cos^2 \Phi + (\sin \Phi - V_{\rm DVR})^2 = V_{\rm source}^2 \tag{1}$$

$$(V_{\text{source}} + V_{\text{DVR}} \cdot \cos \alpha)^2 + (V_{\text{DVR}} \cdot \sin \alpha)^2 = 1$$
(2)

where $V_{\rm DVR}$ and $V_{\rm source}$ are the magnitudes of the injection voltage and the source voltage, respectively. α is the phase difference between their phasors and Φ is the phase difference between the load voltage and load current. Considering (1), it can be concluded that

$$\left|V_{\rm DVR}\right| = \left|\sqrt{\left|V_{\rm source}^2 - \cos^2\Phi\right|} - \sin\Phi\right| \tag{3}$$

Magnitude of injection voltage (V_{DVR}) can be calculated through (3).

Yet α should be determined for the zero energy compensation approach (phase of V_{DVR}) and then generated by inverter. α is calculated from (2) as follows

$$\cos \alpha = \frac{1 - V_{\text{source}}^2 - V_{\text{DVR}}^2}{2V_{\text{source}} \cdot V_{\text{DVR}}}$$
(4)

Hence, three phase locked loops (PLLs) are needed in this scheme. Two PLLs for calculating phase of load voltage and load current; where the difference between them gives the load angle (Φ). The third one estimates phase of the supply voltage, which is considered as phase reference in phasor calculations.

2.2 Benefits and challenges of the multilevel converters

A DVR with conventional converter is displayed in Fig. 2*a*. In addition to the converter, estimation unit, and control stage, the system has a series injection transformer, bypass thyristors and output filters. The two anti-parallel thyristors bypass the DVR terminals when the supply voltage is in normal range to prevent the losses at the DVR and to protect it against the electrical faults. The series injection transformer is a 50/60 Hz transformer and its rated secondary voltage is typically between 20 and 25% of nominal supply voltage. Depending on the compensation method, 10-20% of nominal load power may pass through this transformer during compensation. Assuming there is a power source that could provide this level of power, the transformer would be a bulky element which adds losses to the system.

Fig. 2b illustrates structure of the DVR that is utilised in this paper. This DVR employs a multilevel CHB converter. This type of converter is extremely modular and generates voltage waveforms with small dv/dt and low total harmonic distortion (THD). Moreover, due to series connection of H-bridge cells, it can be easily extended for different voltage and power levels and one can perform fault-tolerant algorithms during the failure of power switches.



Fig. 2 DVR streatures a Conventional DVR b CHB-based DVR

Table 1 Voltage sags recorded in MWPI

No.	Sag depth, %	Sag duration, ms		
1	12.4	40		
2	12.4	50		
3	13.2	60		
4	11.1	50		
5	11.2	30		
6	19.1	50		
7	16.9	70		
8	11.4	350		
9	42.4	60		

A CHB converter with *n* H-bridge cells is able to synthesise 2n + 1 levels at its AC terminals. Due to the synthesised multilevel waveform, the CHB converter needs a small filter on its output terminals to keep the THD within acceptable range [17]. The reduction in size of the output filter leads to lower losses and system costs. Moreover, the converter does not need a series injection transformer to connect it to 20 kV network, which reduces the losses, cost and volume.

During three months of monitoring the supply network of MWPI in 2004, nine voltage sags and one voltage swell were recorded [2]. Table 1 lists details of the voltage sags. It can be seen that the depth of voltage sags are between 10 and 20% of nominal value for eight (out of nine) events. Hence, it seems reasonable to design a DVR which compensates voltage sags with the maximum depth of 20% to decrease the capital investment of the DVR. Regarding this assumption, the DVR should be able to compensate voltage sags with depth of 4 kV. As shown in Fig. 1*c*, in the minimum energy compensation, the magnitude of injected voltage by the DVR is larger than the sag depth. Considering $\cos(\Phi) = 0.9$ in (3) and DC link utilisation of 0.85, the maximum value of V_{DVR} will be 7.25 kV. Therefore, the reference of total DC link voltages (V_{CTRef}) is set to 8 kV. Using six H-bridges in each phase, the reference voltage for each DC link capacitor (V_{CRef}) becomes 1.33 kV. Considering a 25% safety margin, 1700 V IGBTs are a proper choice for this converter. Additionally, the switching frequency of H-bridge cells is limited to 2 kHz in order to decrease the switching loss.

3 Controlling and balancing DC link capacitor voltages

To guarantee proper operation of the CHB converter, voltage of DC link capacitors should always remain close to the reference value [16]. Employing zero energy compensation, net flow of active power between the capacitors and the network would be zero. However, the capacitors and H-bridge cells have internal losses which lead to small discharge currents inside the capacitors and voltage drop. Transients and measurement errors can also lead to flow of active power. Hence, an active voltage balancing algorithm should be implemented to control the voltage of DC link capacitors.

The voltage control scheme, implemented in this research, has two steps: (i) it keeps the total voltage of DC links (V_{CT}) close to the reference value (V_{CTRef}) and (ii) it provides voltage balance among the DC link capacitors. Total DC link voltage is sum of individual DC link voltages, hence

$$V_{\rm CT} = \sum_{i=1}^{6} V_{\rm Ci}$$
 (5)

and

$$V_{\rm CTRef} = 6V_{\rm CRef} \tag{6}$$

where V_{Ci} is DC link voltage of the *i*th cell. Therefore, performing the two steps of the voltage control scheme guarantees correct regulation of DC link voltages. The first step is performed via two controllers: controller I and controller II, which are



Fig. 3 Total DC link voltage is controlled by two controllers *a* Controller I in standby mode

b Controller II in compensation mode



Fig. 4 Flowchart of voltage balancing algorithm in the CHB inverter

displayed in Fig 3. Controller I is active whenever the DVR is in standby mode, and controller II performs the regulation of $V_{\rm CT}$ during compensation period. These controllers keep the total DC link voltage close to the reference value, but cannot maintain voltage balance among DC link voltages. Therefore, a voltage balancing mechanism is also employed to keep the voltage balance, i.e. step 2 of the aforementioned voltage control scheme. This balancing scheme will be discussed in the final part of this section.

Table 3 System parameters under simulation study

Network					
Parameter	Value				
network voltage	20 kV				
load power	35 MW				
load power factor	0.78 inductive				
CHB converter					
voltage of DC link capacitor	1.33 kV				
number of H-bridge cells per phase	6				
line filter inductor	1.1 mH				
line filter capacitor	90 µF				
switching frequency	2 kHz				

Controller I is shown in Fig. 3*a*. It compares V_{CT} with V_{CTRef} and if the difference $(\Delta V_{\rm CT})$ exceeds a predefined margin, it will attempt to bring the DC link voltage, $V_{\rm CT}$, to the acceptable range. If $V_{\rm CT}$ is $<0.95 \times V_{\text{CTRef}}$, controller I turns bypass thyristors off and activates the converter in voltage source mode, with a reference voltage signal which is in-phase with line current; Φ_I in Fig. 3*a* is phase of load current. Therefore, active power flows into the DVR and the capacitors will be charged, raising $V_{\rm CT}$ beyond the lower threshold. If V_{CT} exceeds $1.05 \times V_{CTRef}$, controller I will generate a reference signal opposite in phase with the line current. Therefore, active power will flow from DVR into the network and DC link voltages will drop below the upper threshold. Therefore, controller I is able to control the total DC link voltage when the DVR is in standby mode. Magnitude of the charging/discharging current depends on amplitude of the sinusoidal reference signal. Large charging/discharging current can lead to undesirable voltage drop on the line impedance and filters. On the other hand, small charging/discharging current means slower control of the capacitors and DC link voltages. In this research, amplitude of the voltage reference signal, a in Fig. 3a, is configured in a way that the capacitors get charged from 0 to 100% in \sim 10 cycles.

Fig. 3b displays controller II. This controller is activated during compensation and controls total DC link voltage. During compensation, the voltage signal of the voltage source inverter is perpendicular to line current, preventing exchange of active power between the DVR and the network. However, internal losses could discharge DC link capacitors or cause exchange of small amounts of active power and therefore change the total DC link voltage. In this case, voltages of DC link capacitors should be controlled through small exchange of active power. Controller II performs this task via making small changes in phase of the reference signal of the voltage source inverter, i.e. the reference signal is no longer perpendicular to the line current. This small change leads to exchange of small amounts of active power between DC link capacitors and the network. Fig. 3b displays schematic of controller II, α being phase of the reference voltage signal which is fed to the voltage source inverter. This signal has 90° phase difference with the line current. α' in Fig. 3b is the controlled phase of the reference signal and has a small difference with α . This difference leads to flow of active power between the network and the DVR.

 Table 2
 DVR performance comparison between previous studies and the current study

Study	Converter type	Medium voltage (MV) connection	Energy storage	Switching frequency	Voltage balance	Unbalanced compensation	Size of line filter	Harmonic mitigation
[7]	2-level	transformer	batteries	high	_	no	medium	no
[8]	2-level	transformer	batteries	high	_	no	medium	yes
[9]	matrix	transformer	grid	high	_	no	medium	no
[10]	AC–AC, buck, boost	transformer	grid	high	-	no	medium	no
[11]	2-level, AC-AC	transformer	grid	high	_	no	medium	no
[12]	CHB	direct	batteries	low	_	yes	small	yes
[13]	CHB, DC-DC	direct	batteries	low	_	no	small	no
[14, 15]	ĊHB	direct	capacitors	low	no	ves	small	no
current	CHB	direct	capacitors	low	yes	yes	small	yes
study			-					-



Fig. 5 Three-phase voltage sag

a Network voltage

b Injected voltage by the DVR

c Load-side voltage

The second step of the voltage control scheme is performed through a balancing mechanism introduced in [13, 14]. The original scheme [18, 19] was designed for a rectifier, but with some modifications, it has been adopted for the converter in this research which works in both rectifier and inverting modes. In this scheme, participation of H-bridge cells in synthesising a voltage level is decided based on two rules: (i) the line current being charging or discharging; and (ii) which cells need to be charged and which ones need to be discharged. Three modes are defined for H-bridge cells: '+1', '0' and 'PWM'. In '+1' mode, the AC terminal voltage



Fig. 7 Unbalanced voltage sag (a 20% voltage sag on phase A) a Source voltage

b Injected voltage by the DVR

c Load-side voltage

of an H-bridge cell is equal to DC link voltage V_{CRef} . In '0' mode, the AC terminal voltage is zero and the cell does not participate in the modulation. In 'PWM' mode, the cell operates in PWM mode and its command is derived by comparing the reference DVR voltage, V^*_{DVR} with the medium frequency carrier signal in the *k*th region, i.e. where $(k - 1)V_{\text{CRef}} \le |V^*_{\text{DVR}}| \le kV_{\text{CRef}}$.

According to demonstrated flowchart in Fig. 4, at the beginning of each balancing period, this method sorts the H-bridge cells based on their DC link voltages. Operating mode of each cell depends on its rank in the sorting and the voltage level that is to be synthesised.



Fig. 6 Voltages of the DC link capacitors



Fig. 8 Three-phase 20% voltage sag with voltage harmonics a Network voltage

b Injected voltage by the DVR

c Load-side voltage

It is worth noting that in the *k*th region, voltage level changes between $(k-1)V_{CRef}$ and kV_{CRef} , where k=1, 2, ..., n. In case of charging current, the (k-1) cells with the lowest voltage, i.e. the ones which need charge are selected to operate in '+1' mode, the *k*th cell in 'PWM' and the rest in '0' mode. On the other hand, if the current is discharging, the (k-1) cells with the highest voltage must be discharged by working in '+1' mode, the *k*th cell in 'PWM' and the rest in '0' mode. For example, to synthesise a voltage between $3V_{CRef}$ and $4V_{CRef}$ when the current is charging, three cells with the lowest voltage are selected to operate in '+1' mode, the fourth one in 'PWM' mode and the rest in '0' mode. Using this strategy, not only is the DVR voltage synthesised, but also the DC link capacitors are balanced.

4 Estimation method

Estimation of amplitude and phase of sinusoidal three-phase voltages and currents is an important issue in many PQ applications [20], including the DVR introduced in this paper. Accuracy and settling time delay are the key parameters in assessment of estimation methods. Most applications employ Park transform and fast Fourier transform (FFT) methods for estimation of sinusoidal waveforms. FFT estimates parameters of a sinusoidal waveform based on a window of samples. It has good accuracy, and its delay





Fig. 9 Block diagram and test setup of the prototype *a* Schematics of the laboratory-scale prototype *b* Picture of test setup

depends on length of the sampling window. Following a change in amplitude or phase of the sinusoidal waveform, FFT output will reach steady state when all of the samples have been updated. Park transform uses instantaneous values for estimation. Park transform considers a synchronous rotating frame with two axes called Dand Q. D and Q elements of a three phase system are calculated through (7). High accuracy and small delay of Park transform are desirable, but it can only estimate balanced three-phase systems. Additionally, its dynamic behaviour is highly dependent on behaviour of the PLL implemented in it. However, Park transform is still employed in several applications, including active power filters [21], electrical machine control [22] and sub-synchronous oscillations [23] (see (7))

 V_q , V_d and V_z in (7) are *D*, *Q* and DC elements of the three-phase system comprised of V_a , V_b and V_c , respectively.

The estimation method employed for simulation study (in this paper) is based on [23]. It uses Park transform and theory of positive, negative and zero sequences [24]. It calculates phase and magnitude of the sequences, and then estimates phase and magnitude of each phase independently under balanced and

$$\begin{bmatrix} V_q(t) \\ V_d(t) \\ V_z(t) \end{bmatrix} = \frac{2}{3} \times \begin{bmatrix} \sin(\omega t) & \sin(\omega t - 2\pi/3) & \sin(\omega t + 2\pi/3) \\ \cos(\omega t) & \cos(\omega t - 2\pi/3) & \cos(\omega t + 2\pi/3) \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \times \begin{bmatrix} V_a(t) \\ V_b(t) \\ V_c(t) \end{bmatrix}$$
(7)

Parameter	Value		
nominal network voltage	50 V		
switching frequency	2 kHz		
nominal DC link voltage	10 V		
number of series H-bridges	3		
line filter inductor	4 mH		
line filter capacitor	60 µF		
load power	12 VA		
load power factor	0.7 capacitive		

unbalanced conditions. Employing several delay elements, this method successfully eliminates the high order sinusoidal disturbances in output of Park transform that originate from imbalances.

Finally to compare the performance of the proposed multilevel DVR and its control strategy with the previous approaches, a comparison is carried out and is given in Table 2.

5 Simulation results

Three simulation scenarios are defined and performed to assess the performance of the new DVR under different voltage sags.

Table 3 lists parameters of the simulation. The network voltage and load are selected similar to the MWPI network. Therefore, these scenarios assess the performance of the proposed DVR in mitigation of voltage sags that occur on MWPI supply network. The parameters of the designed DVR are shown in Table 3. The simulations are performed in PSCAD/EMTDC environment and the results are presented in the following sections.

5.1 Three-phase voltage sag

A three-phase balanced voltage sag with depth of 20% occurs at t=0.2 s and lasts for ten fundamental cycles. Fig. 5 shows network voltage, DVR voltage and restored supply voltage. It can be observed in Fig. 5*c* that the load supply voltage has been restored to its normal range in less than half a cycle. THD of this voltage is 4%, which is within the range specified in network codes (maximum 5%). Thus, performance of the compensation control is confirmed here.

Fig. 6 illustrates individual voltages of the DC link capacitors of one phase. The voltage balance between individual capacitors is well provided. Additionally, the ripple of DC link voltages is lower than $\pm 10\%$ and the ripple frequency is $2f_0$; where f_0 is the fundamental frequency of the network, i.e. 50 Hz. Therefore, the voltage control scheme is working well.



Fig. 10 Experimental investigation of the DVR performance (on the left); and results of simulation with the same parameters (on the right)



Fig. 11 DVR AC terminal voltage and line current: experimental results (on the left); and results of simulation with the same parameters (on the right)



Fig. 12 Investigating the performance of the voltage balance controller

5.2 Single-phase voltage sag

This simulation scenario is designed to assess performance of the proposed DVR in estimation and restoration of unbalanced voltage sags. In this scenario, a voltage sag with depth of 20% occurs at t=0.2 s on phase A, and lasts for five cycles. Fig. 7 shows the network voltage, DVR voltage and restored supply voltage. It demonstrates that the DVR can successfully distinguish and mitigate unbalanced voltage sags.

5.3 Three-phase voltage sag with voltage harmonics

In this simulation, capability of the proposed DVR is assessed in presence of voltage harmonics. Fig. 8*a* shows the network voltage. A three-phase voltage sag with depth of 20% occurs at t=0.2 s and lasts for five cycles. Along with the voltage sag, 5th and 7th harmonics are added (7 and 5%, respectively). Figs. 8*b* and *c* show DVR voltage and restored supply voltage, respectively. In

these results, the drop in first harmonic is restored in less than half a cycle, while higher order harmonics are mitigated after one and a half cycle; i.e. the voltage magnitude is restored to the nominal range in <10 ms, while the THD settles within admissible range after 30 ms. This scenario not only demonstrates capability of the proposed DVR in exact estimation and restoration of the first harmonic in presence of higher harmonics, but also approves its performance in mitigation of voltage harmonics.

6 Experimental results

A laboratory-scale prototype of the proposed DVR has been built and used to assess the DVR performance in practice. Due to the limited facilities, it was not possible to perform the experimental tests on a high-power prototype. The implemented DVR is based on a single-phase 7-level CHB inverter. Block diagram and test setup of the prototype is depicted in Fig. 9. Fig. 9b displays the complete test setup, including digital signal processor (DSP)



Fig. 13 DC link voltages during compensation: experimental results (on the left); and results of simulation with the same parameters (on the right)

controller and its interface, line filters, a CHB inverter with three cells and the load. The DSP controller is a TMS320F28335 TI processor. Input signals, i.e. output of voltage and current sensors are fed to the DSP via an interface circuit. Output of the DSP, i.e. gate commands also pass through the interface and reach the CHB converter cells. In order to better justify the experimental verification, a simulation was also performed with parameters similar to the prototype.

Table 4 lists parameters of the test setup and the simulation. Since the test is done on a single-phase system, the estimation method introduced in Section 4 was not applicable, and instead of it, a 24-sample full-window FFT estimation unit was implemented. Therefore, this test is only capable of assessing the proposed compensation and voltage control schemes.

During the test, a 20% voltage sag was generated on the network voltage, which lasted for ~9 cycles. The network voltage, DVR voltage and load supply voltage are illustrated in Fig. 10. Additionally, Fig. 11 shows the 7-level DVR voltage (before its output filter) along with line current during the voltage sag. Here, 90° phase difference can be clearly seen between them. Therefore, zero energy compensation method has been well performed.

Figs. 12 and 13 demonstrate the performance of voltage control scheme. Fig. 12 shows DC link voltages when the voltage balance controller is on or off. Different resistors were installed in parallel with each DC link capacitor in order to intensify the imbalance between them, hence, diverging DC link voltages. When the controller is on, the voltage balance controller successfully converges the DC link voltages to their nominal value. Fig. 13 shows the DC link voltages along with the load voltage under voltage sag condition and assures that voltage control is well performed during compensation.

7 Conclusions

This paper presented design and performance assessment of a DVR based on the voltage sag data collected from MWPI. Using a multilevel converter, the proposed DVR was capable of direct connection to the medium voltage-level network without a series injection transformer. In addition, development of zero active power compensation technique helps to achieve voltage restoration goal just by the capacitors as energy storages. Due to internal losses of H-bridge cells and probable inaccuracies in measurements, voltage of DC link capacitors may become unequal, which prevents proper operation of the converter. A voltage control scheme, comprised of three separate controllers, was proposed in this paper for keeping voltage balance among the DC link capacitors within nominal range. A fast estimation method was also employed for calculation of phase and magnitude terms in an unbalanced three-phase system. This estimation method is able to recognise voltage sags in approximately half a cycle. Several simulations were performed in PSCAD/EMTDC environment to verify the performance of CHB-based DVR. Additionally, a laboratory-scale prototype of the proposed DVR was built and tested. Results of the experimental test also confirmed validity of the proposed control system.

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References 9

- 1 Chapman, D.: 'The cost of poor power quality' (European Copper Institute, Copper Development Association, 2001), March Radmehr, M., Farhangi, S., Nasiri, A.: 'Effects of power quality distortions on
- electrical drives and transformer life in paper industries', IEEE Ind. Appl. Mag., 2007, 13, (5), pp. 38-48
- Lamoree, J., Mueller, D., Vinett, P.: 'Voltage sag analysis case studies', IEEE 3
- *Trans. Ind. Appl.*, 1994, **30**, (4), pp. 1083–1089 Bollen, M.H.J.: 'Understanding power quality problems: voltage sags and interruptions' (New York, Saranarce University of Technology, 2000)
- Ghosh, A., Ledwich, G.: 'Power quality enhancement using custom power devices' (Berlin, Kluwer Academic Publications, 2002)
- Nielsen, J.G., Newman, M., Nielsen, H., et al.: 'Control and testing of a dynamic voltage restorer (DVR) at medium voltage level', IEEE Trans. Power Electron., 2004, 19, (3), pp. 806-813
- Huang, C.J., Huang, S.J., Pai, F.S.: 'Design of dynamic voltage restorer with disturbance-filtering enhancement', IEEE Trans. Power Electron., 2003, 18, (5), pp. 1202-1210
- Newman, M.J., Holmes, D.G., Blaabjerg, F.: 'A dynamic voltage restorer (DVR) with selective harmonic compensation at medium voltage level', IEEE Trans. Ind. Appl., 2005, 41, (6), pp. 1744-1753
- Lozano-Garcia, J.M., Ramirez, J.M.: 'Voltage compensator based on a direct matrix converter without energy storage', *IET Power Electron.*, 2015, **8**, (3), pp. 321-332
- Kwon, J.M., Kim, K.T., Kwon, B.H.: 'Instant voltage compensator based on a 10 three-leg converter', IET Power Electron., 2013, 6, (8), pp. 1618-1625
- 11 Rosas-Caro, J.C., Mancilla-David, F., Ramirez-Arredondo, J.M., et al.: 'Two-switch three-phase ac-link dynamic voltage restorer', IET Power Electron., 2012, **5**, (9), pp. 1754-1763 Chen, G., Zhu, M., Cai, X.: 'Medium-voltage level dynamic voltage
- 12 restorer compensation strategy by positive and negative sequence extractions in multiple reference frames', *IET Power Electron.*, 2014, 7, (7), pp. 1747–1758 Babaei, E., Kangarlu, M.F., Sabahi, M.: 'Dynamic voltage restorer based on
- 13 multilevel inverter with adjustable dc-link voltage', IET Power Electron., 2014,
- 7, (3), pp. 576–590 Al-Hadidi, H.K., Gole, A.M., Jacobson, D.A.: 'A novel configuration for a cascade 14 inverter-based dynamic voltage restorer with reduced energy storage requirements', IEEE Trans. Power Deliv., 2008, 23, (2), pp. 881-888
- Al-Hadidi, H.K., Gole, A.M., Jacobson, D.A.: 'Minimum power operation of 15 cascade inverter-based dynamic voltage restorer', IEEE Trans. Power Deliv., 2008, 23, (2), pp. 889-898
- Galeshi, S., Imaneini, H.: 'A fast estimation method for unbalanced three-phase 16 systems', Fourth Power Electronics, Drive Systems and Technologies Conf. (PEDSTC 2013), February 2013, pp. 383–388 Rodriguez, J., Franquelo, L.G., Kouro, S.: 'Multilevel converters: an
- 17 enabling technology for high-power applications'. Proc. IEEE, 2009, vol. 97, pp. 1786–1817
- Iman-Eini, H., Schanen, J.L., Farhangi, S., *et al.*: 'A modular strategy for control and voltage balancing of cascaded H-bridge rectifiers', *IEEE Trans. Power* 18 *Electron.*, 2008, **23**, (5), pp. 2428–2442 Iman-Eini, H., Schanen, J.L., Farhangi, S., *et al.*: 'Design of cascaded H-bridge
- 19 rectifier for medium voltage applications'. PESC, 2007, pp. 653-658
- 20 Cease, T.W., Feldhaus, B.: 'Real-time monitoring of the TVA power system', IEEE
- 21
- Comput. Appl. Power, 1994, 7, (3), pp. 47–51 Akagi, H.: 'Active harmonic filters', *Proc. IEEE*, 2005, **93**, (12), pp. 2128–2141 Adkins, B.: 'The general theory of electrical machines' (Wiley, New York, 1957) Anderson, P.M., Agrawal, B.L., Van Ness, J.E.: 'Subsynchronous resonance in power systems' (IEEE, New York, 1990) 22 23
- 24 Kimbark, E.: 'Solution of faulted three-phase networks' (Wiley-IEEE, 1995)